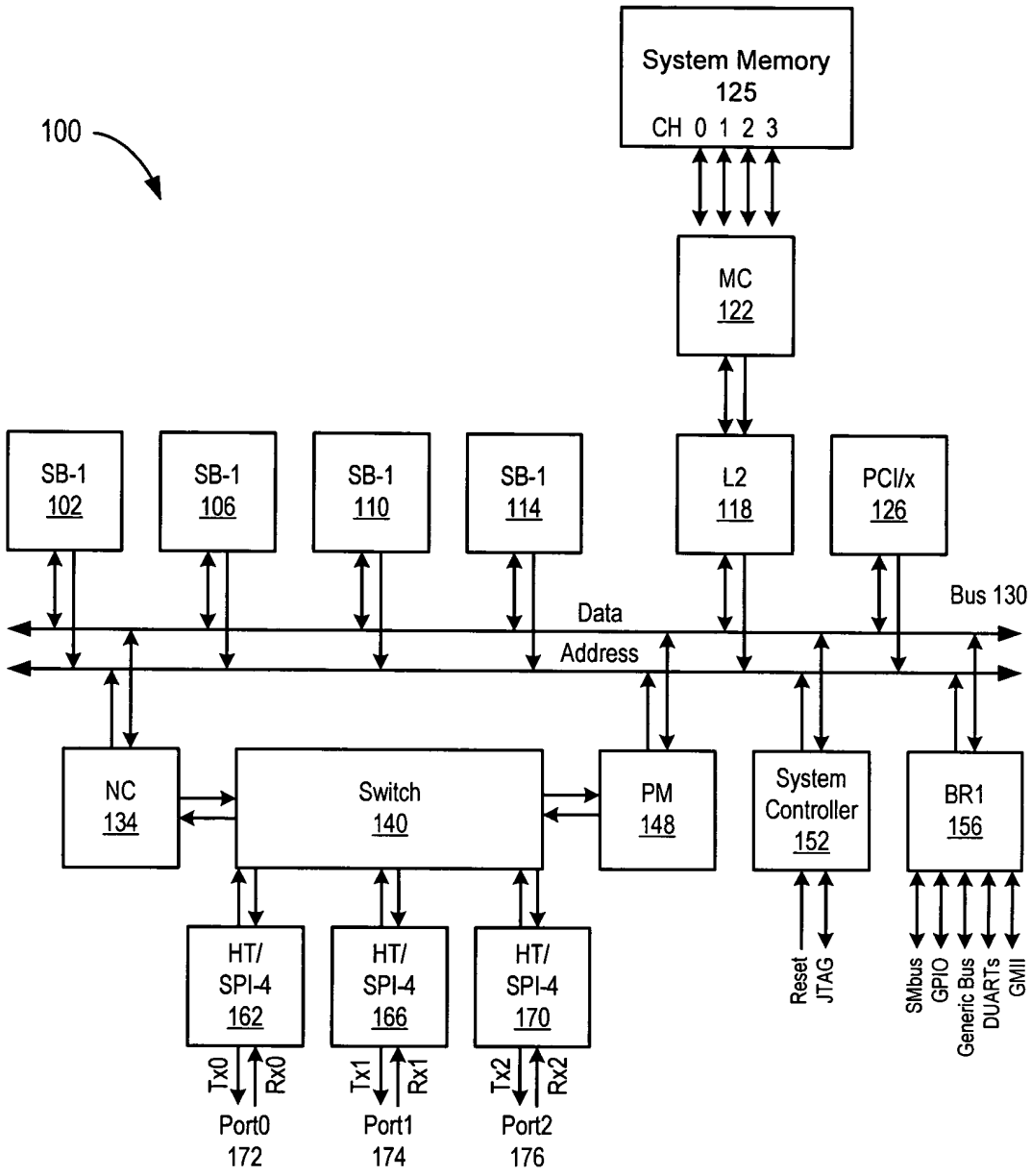
100
System Memory
125
CH 0 1 2 3
MC
122
SB-1
102
SB-1
106
SB-1
110
SB-1
114
L2
118
PCI/x
126
Bus 130
Data
Address
NC
134
Switch
140
PM
148
System
Controller
152
BR1
156
HT/
SPI-4
162
HT/
SPI-4
166
HT/
SPI-4
170
Tx0
Rx0
Tx1
Rx1
Tx2
Rx2
Port0
172
Port1
174
Port2
176
Reset
JTAG
SMbus
GPIO
Generic Bus
DUARTs
GMII

Figure 1

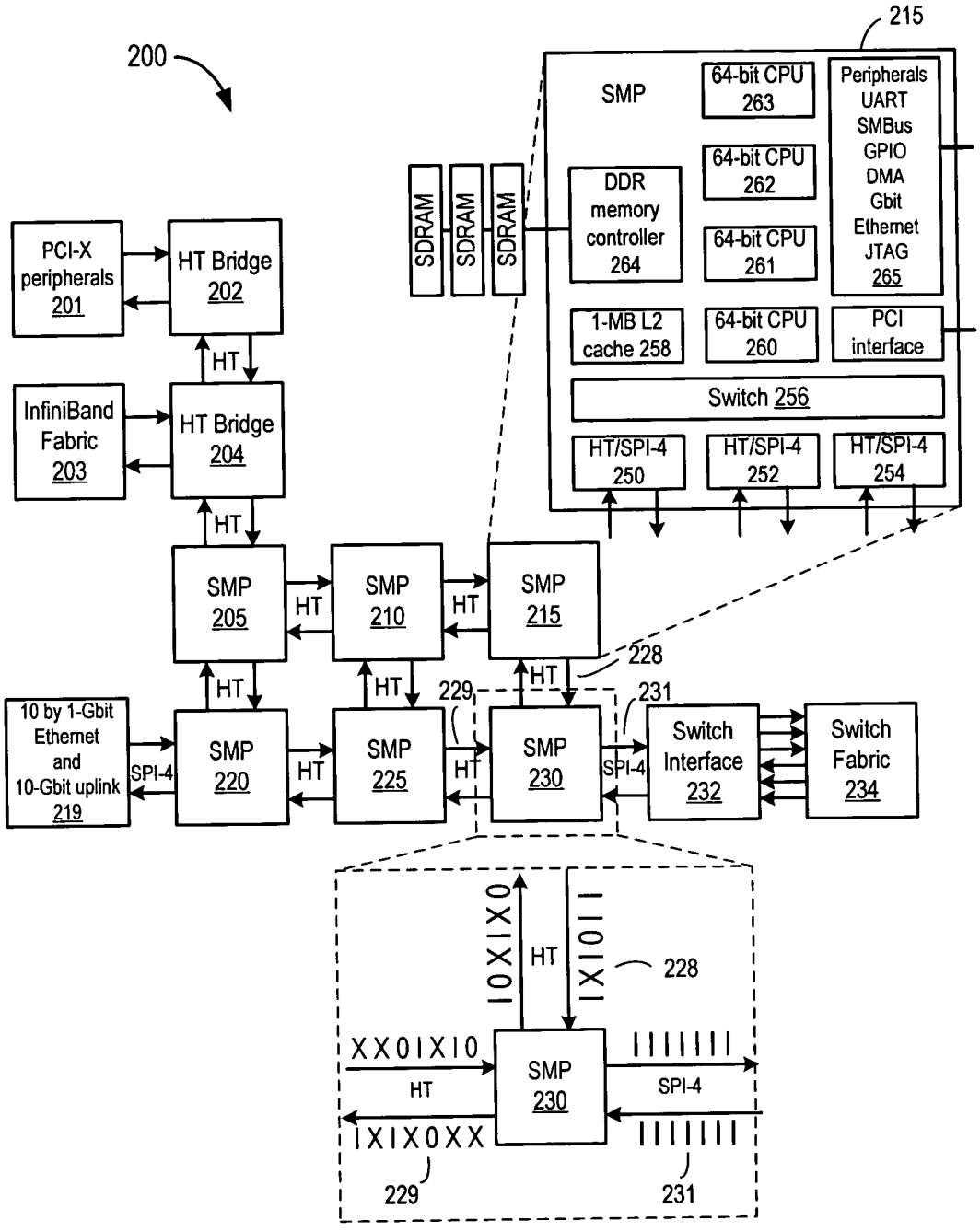
200
215
SMP
64-bit CPU 263
64-bit CPU 262
64-bit CPU 261
64-bit CPU 260
Peripherals UART SMBus GPIO DMA Gbit Ethernet JTAG 265
DDR memory controller 264
SDRAM
SDRAM
SDRAM
1-MB L2 cache 258
PCI interface
Switch 256
HT/SPI-4 250
HT/SPI-4 252
HT/SPI-4 254
PCI-X peripherals 201
HT Bridge 202
InfiniBand Fabric 203
HT Bridge 204
HT
SMP 205
SMP 210
SMP 215
228
229
231
10 by 1-Gbit Ethernet and 10-Gbit uplink 219
SPI-4
SMP 220
SMP 225
SMP 230
Switch Interface 232
Switch Fabric 234
10XIX0
IIOIXI
XX0IX10
IXIX0XX
IIIIIIII

Figure 2

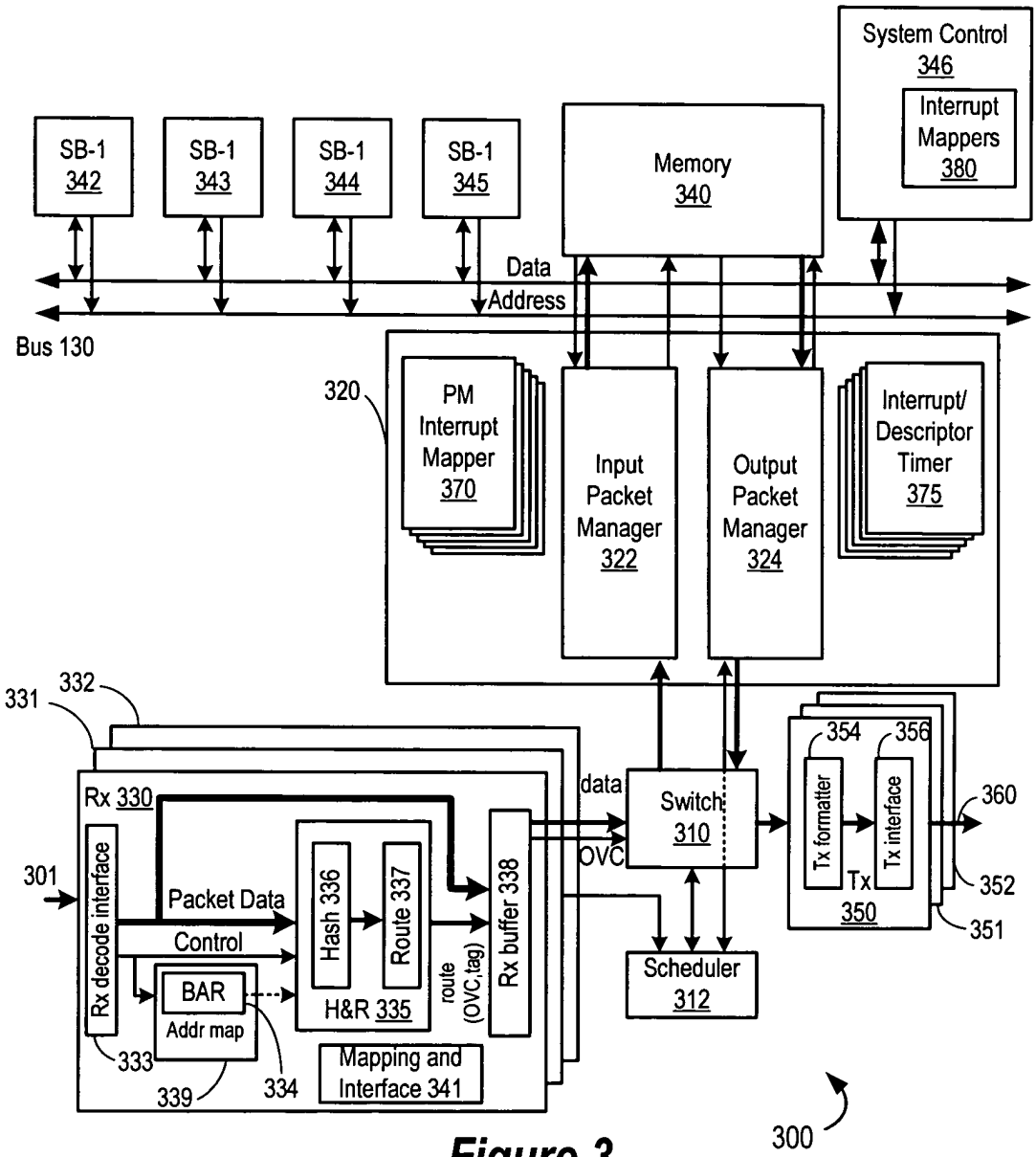
System Control
346
Interrupt
Mappers
380
SB-1
342
SB-1
343
SB-1
344
SB-1
345
Memory
340
Data
Address
Bus 130
320
PM
Interrupt
Mapper
370
Input
Packet
Manager
322
Output
Packet
Manager
324
Interrupt/
Descriptor
Timer
375
331
332
Rx 330
301
Rx decode interface
Packet Data
Control
BAR
Addr map
333
339
334
Hash 336
Route 337
H&R 335
route
(OVC,tag)
Rx buffer 338
Mapping and
Interface 341
data
OVC
Switch
310
Scheduler
312
354
356
Tx formatter
Tx interface
Tx
350
360
352
351
300

Figure 3

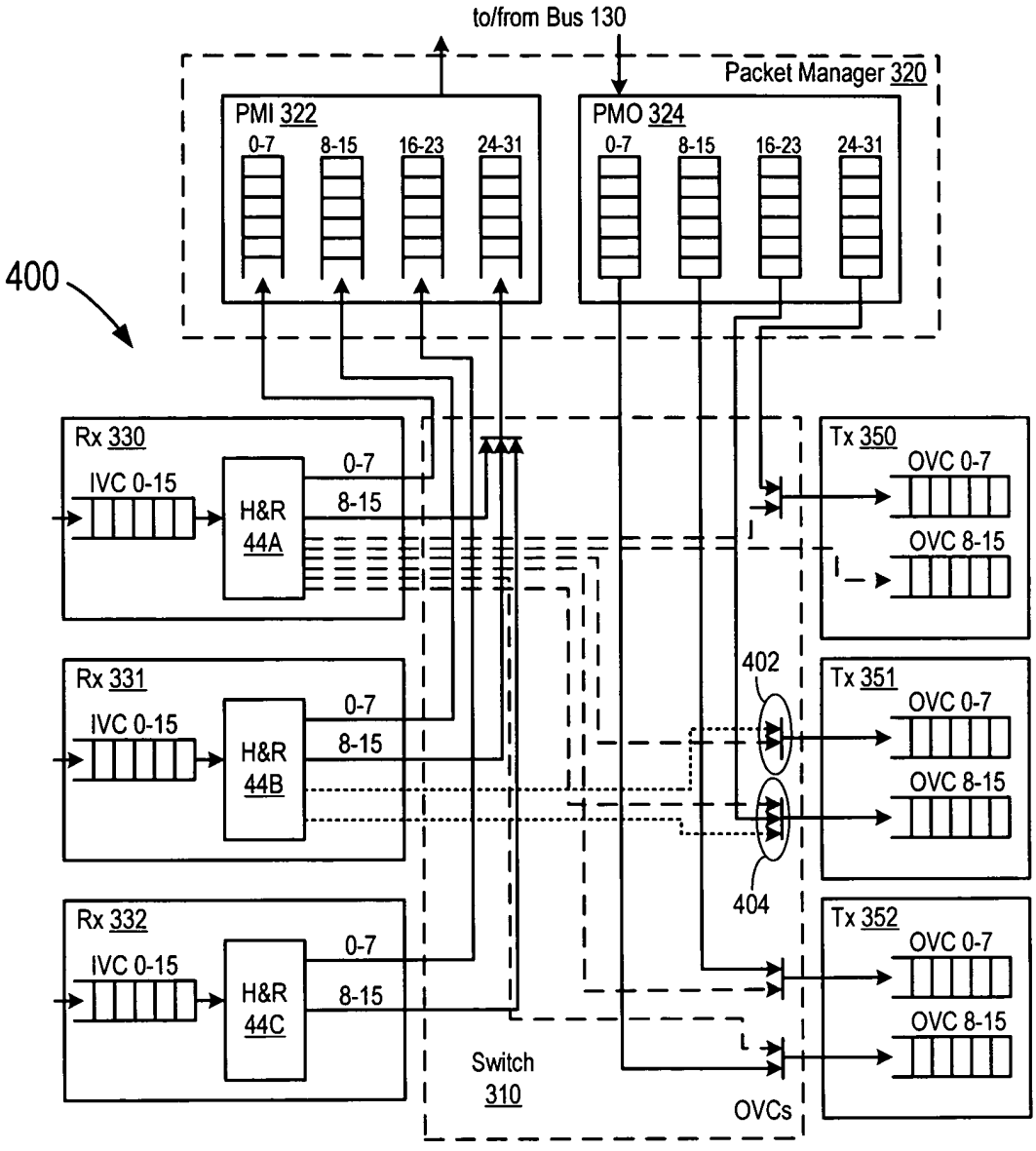
to/from Bus 130
Packet Manager 320
PMI 322
0-7
8-15
16-23
24-31
PMO 324
0-7
8-15
16-23
24-31
400
Rx 330
IVC 0-15
H&R
44A
0-7
8-15
Rx 331
IVC 0-15
H&R
44B
0-7
8-15
Rx 332
IVC 0-15
H&R
44C
0-7
8-15
Switch
310
OVCs
Tx 350
OVC 0-7
OVC 8-15
Tx 351
OVC 0-7
OVC 8-15
Tx 352
OVC 0-7
OVC 8-15
402
404

Figure 4

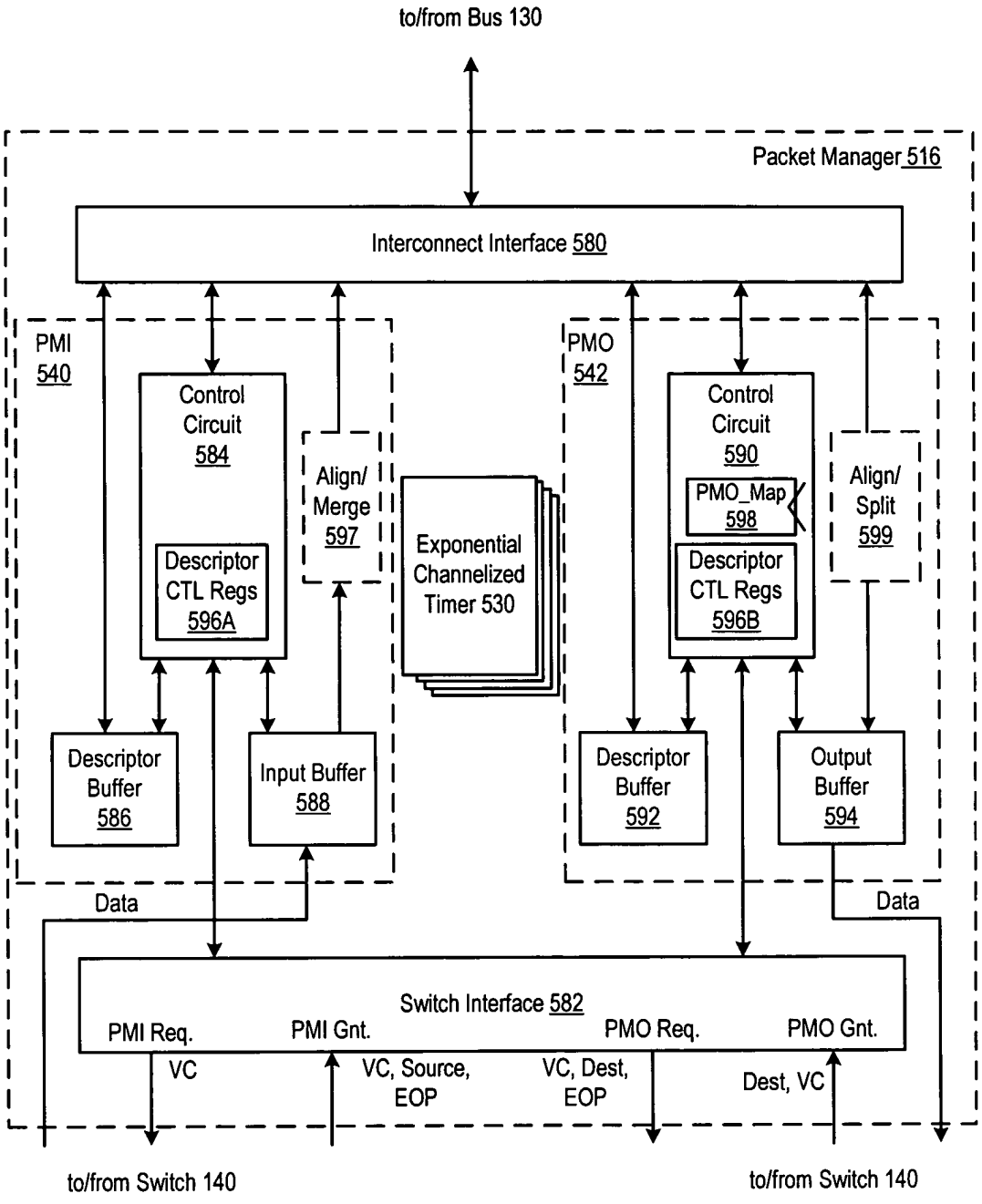
to/from Bus 130
Packet Manager 516
Interconnect Interface 580
PMI
540
Control
Circuit
584
Descriptor
CTL Regs
596A
Align/
Merge
597
Exponential
Channelized
Timer 530
PMO
542
Control
Circuit
590
PMO_Map
598
Descriptor
CTL Regs
596B
Align/
Split
599
Descriptor
Buffer
586
Input Buffer
588
Descriptor
Buffer
592
Output
Buffer
594
Data
Data
Switch Interface 582
PMI Req.
PMI Gnt.
PMO Req.
PMO Gnt.
VC
VC, Source,
EOP
VC, Dest,
EOP
Dest, VC
to/from Switch 140
to/from Switch 140

Figure 5

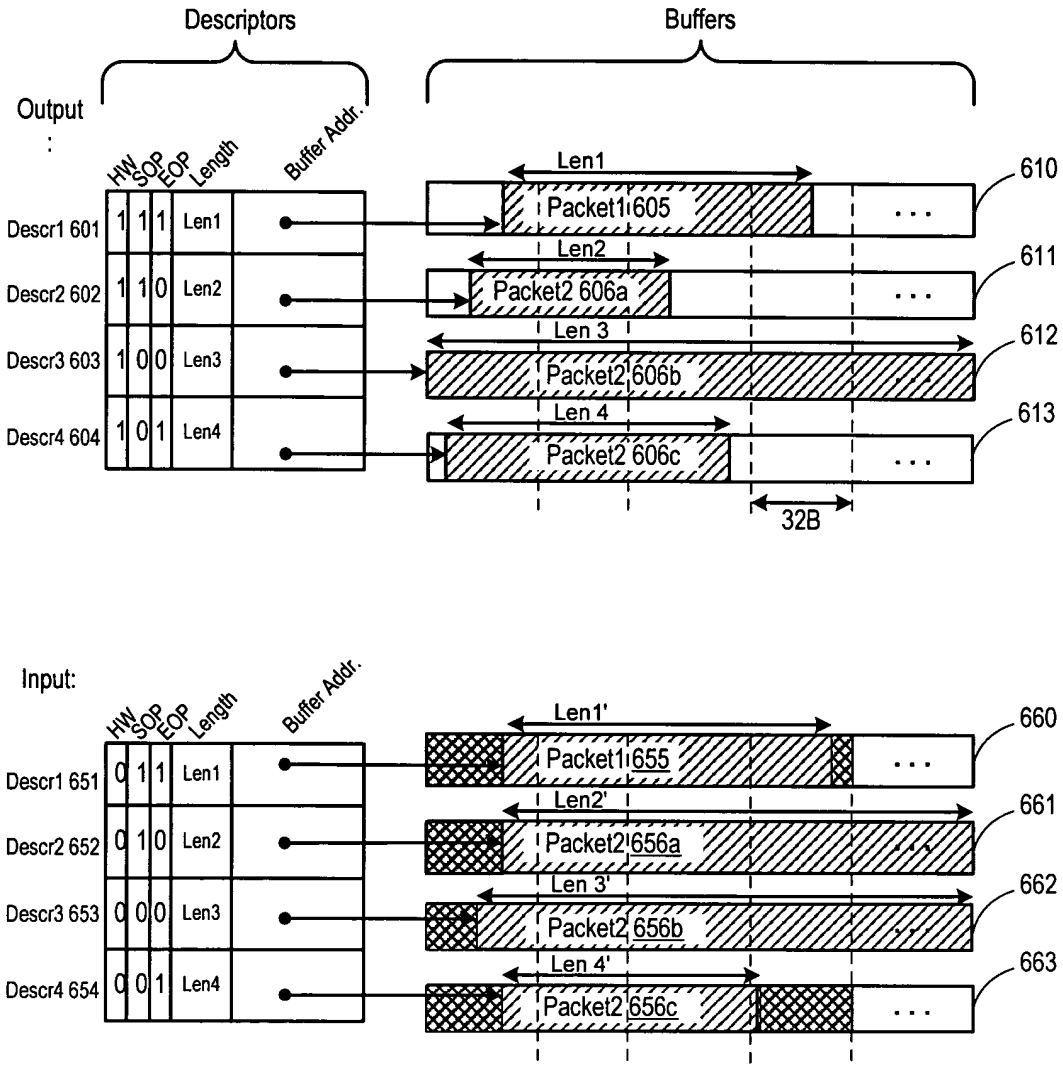
Descriptors
Buffers
Output
HW
SOP
EOP
Length
Buffer Addr.
Descr1 601
Descr2 602
Descr3 603
Descr4 604
Len1
Len2
Len3
Len4
Packet1 605
Packet2 606a
Packet2 606b
Packet2 606c
610
611
612
613
32B
Input:
Descr1 651
Descr2 652
Descr3 653
Descr4 654
Len1'
Len2'
Len 3'
Len 4'
Packet1 655
Packet2 656a
Packet2 656b
Packet2 656c
660
661
662
663

Figure 6

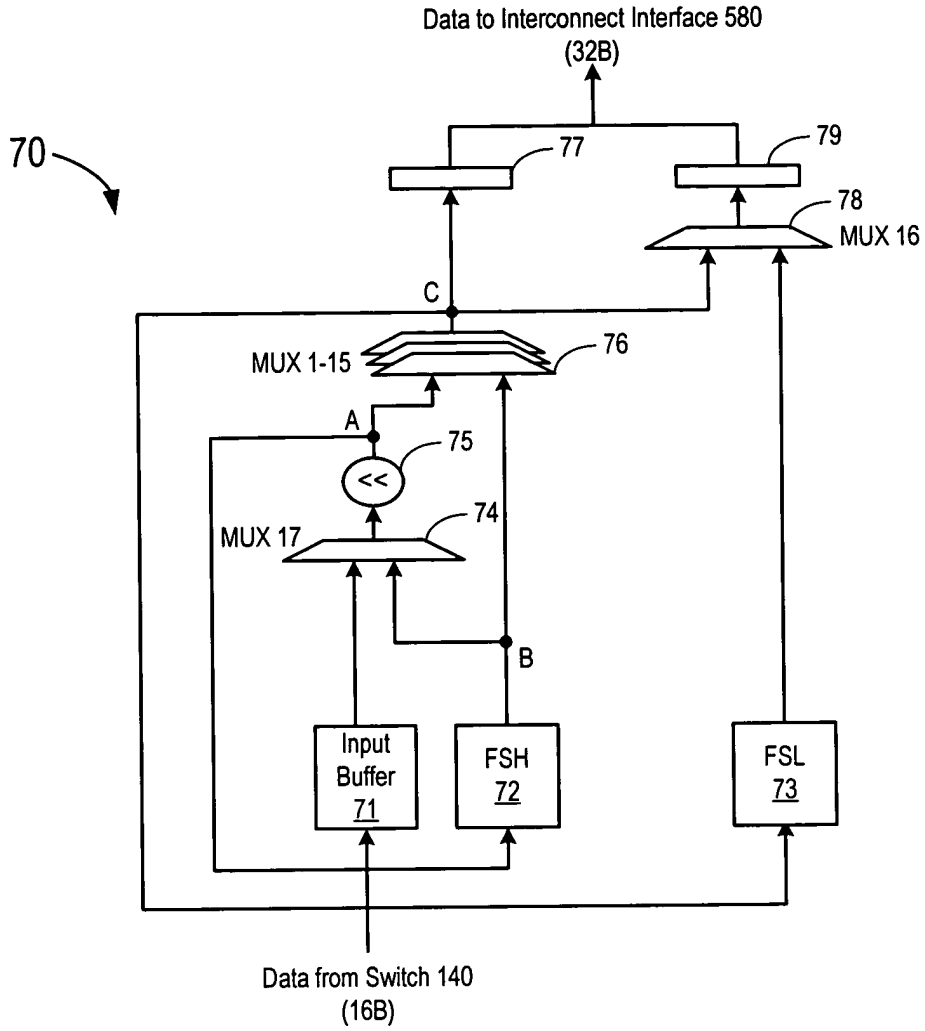
Data to Interconnect Interface 580
(32B)
70
77
79
78
MUX 16
C
MUX 1-15
76
A
75
<<
MUX 17
74
B
Input
Buffer
71
FSH
72
FSL
73
Data from Switch 140
(16B)

Figure 7

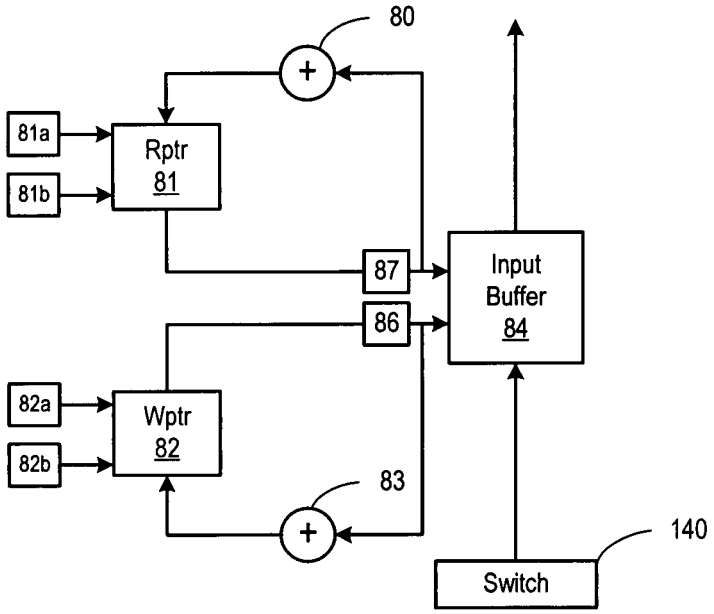

Figure 8

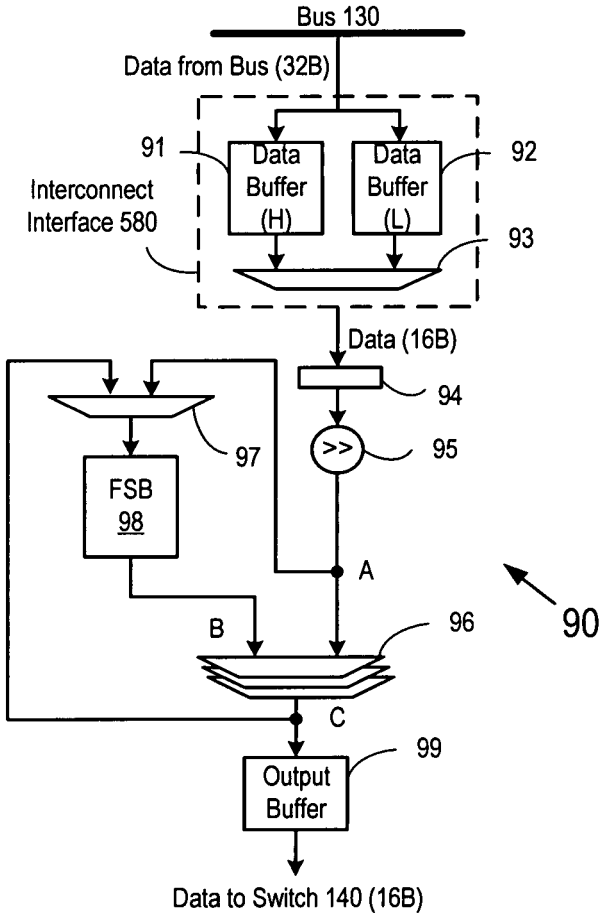

Figure 9

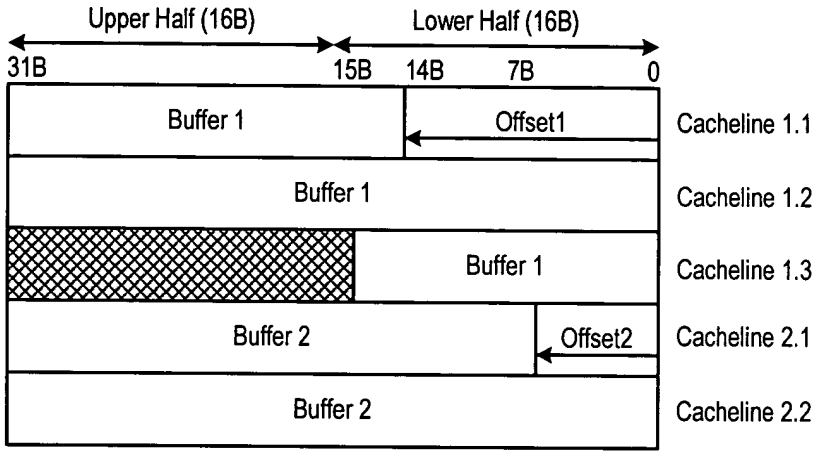

Figure 10

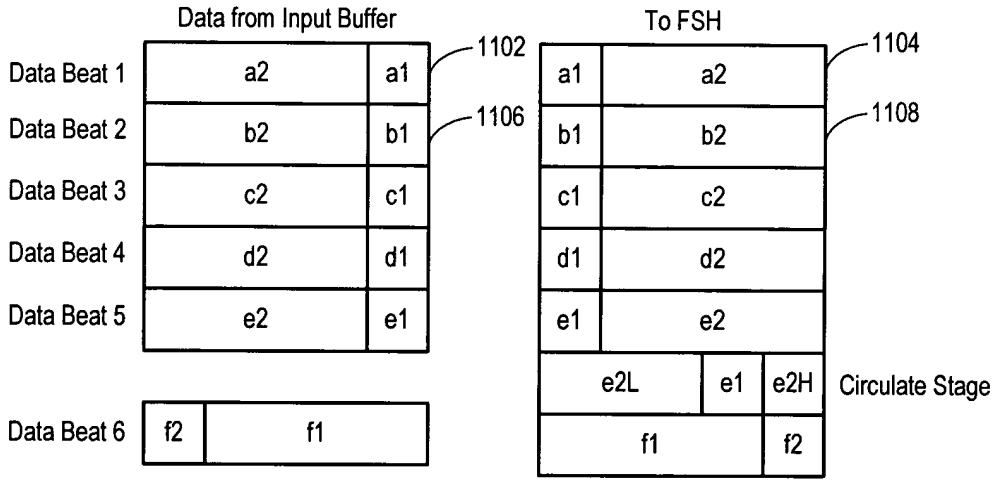

Figure 11

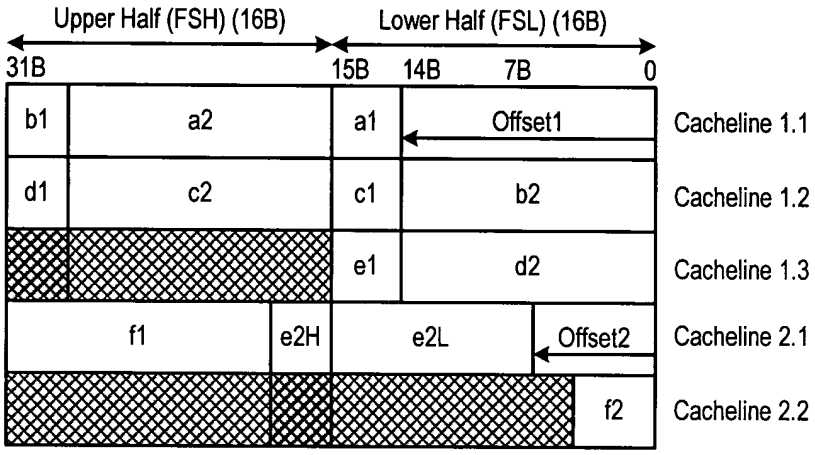
Upper Half (FSH) (16B)
Lower Half (FSL) (16B)
31B
15B
14B
7B
0
b1
a2
a1
Offset1
Cacheline 1.1
d1
c2
c1
b2
Cacheline 1.2
e1
d2
Cacheline 1.3
f1
e2H
e2L
Offset2
Cacheline 2.1
f2
Cacheline 2.2

Figure 12